23. (New) A manufacturing method of a semiconductor memory device having a memory cell array portion and a peripheral transistor portion, said memory cell array portion having a source area formed by a self-aligned process, comprising:

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forming an isolation insulating film on a semiconductor substrate, said isolation insulating film having a plurality of openings, each of said openings having a rectangular shape being elongate in a first direction, said openings being arranged in a second direction crossing said first direction;

forming tunnel insulating films on said semiconductor substrate in said openings;

forming a plurality of word lines on said isolation insulating film and said tunnel insulating films, each of said word lines being elongate in said second direction, said word lines being arranged in said first direction, and forming a plurality of floating gates sandwiched between said word lines and said tunnel insulating films, said floating gates being arranged at intersections of said openings and said word lines, wherein said plurality of word lines comprise at least a first word line and a second word line arranged on the same tunnel insulating films, and wherein said plurality of word lines provide said source area sandwiched between said first word line and said second word line, and a drain area disposed on the other side of said first word line than a side of said source area and disposed on the other side of said second word line than a side of said source area;

removing said isolation insulating film and said tunnel insulating film at said source area to expose said semiconductor substrate having an uneven surface, while said isolation insulating film and said tunnel insulating films are kept on said semiconductor substrate at said drain area;

forming a mask on said source area having said uneven surface;

covering said semiconductor substrate at least at said peripheral transistor portion with a metal film and performing a heat treatment to form a silicide film on said peripheral transistor portion.

24. (New) The method as claimed in claim 23, wherein said mask is formed in a thickness so that a space between said mask on a side surface of said first word line and said mask on a side surface of said second word line facing said side surface of said first word line is left while a surface of said source area is covered with said mask.

25. (New) The method as claimed in claim 24, wherein said mask covers said surface of said source area and top surfaces of said first and second word lines, during the step of covering said semiconductor substrate with said metal film.

26. (New) The method as claimed in claim 24, wherein said mask covers said surface of said source area and

wherein said top surfaces of said first and second word lines are free from said mask, during the step of covering said semiconductor substrate with said metal film.

27. (New) The method as claimed in claim 23, wherein said mask is formed such that a space between a side surface of said first word line and a side surface of said second word line facing with said side surface of said first word line is filled with said mask.

28. (New) The method as claimed in claim 27, wherein said mask covers said surface of said source area and top surfaces of said first and second word lines, during the step of covering said semiconductor substrate with said metal film.

29. (New) The method as claimed in claim 28, wherein said mask consists of one layer.

30. (New) The method as claimed in claim 29, wherein a step of forming said mask comprises:

forming a first mask so that said space is left; and then

forming a second mask so that said space is filled with said second mask, wherein said mask comprises said first mask and said second mask.